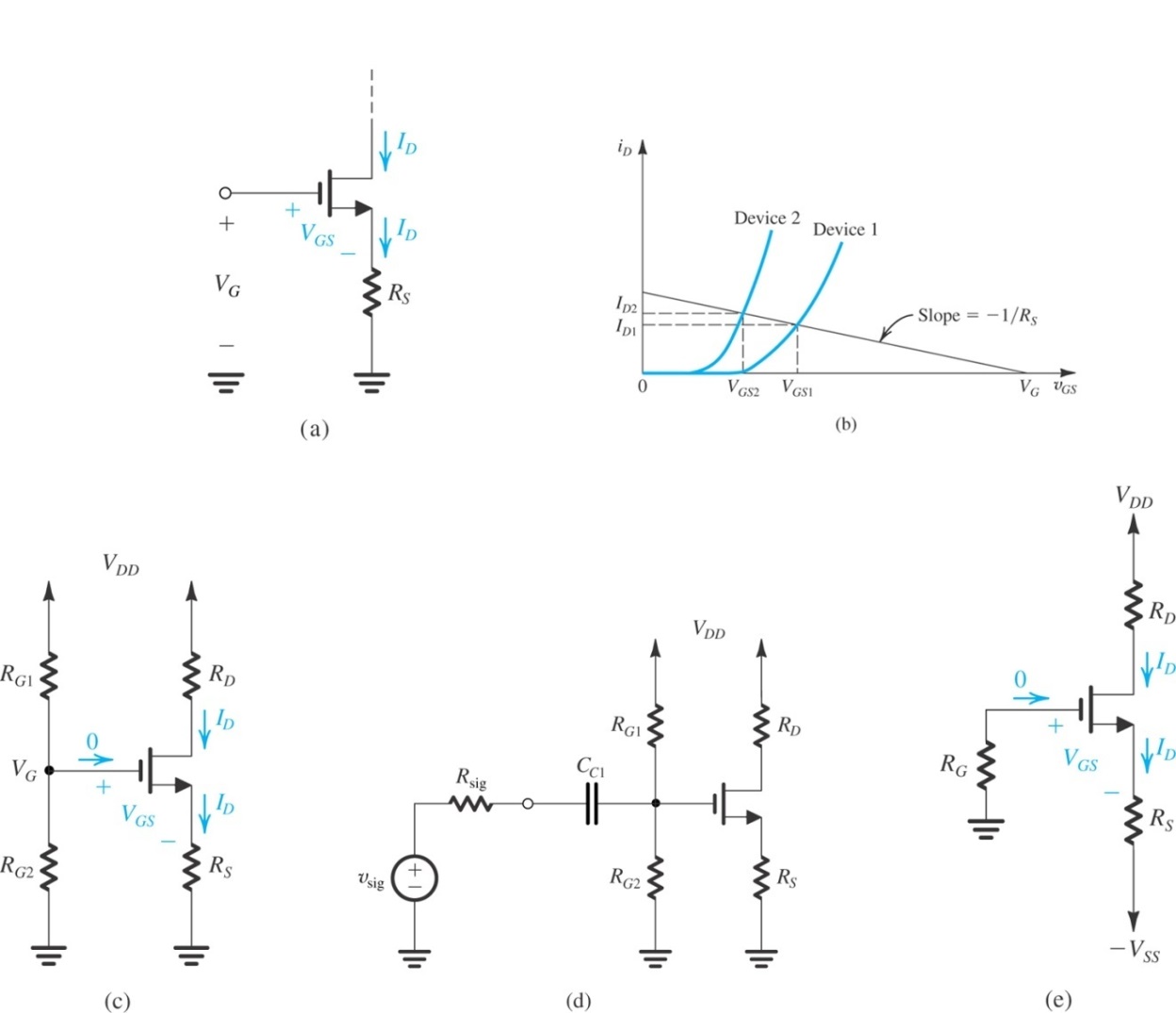
ELEG 309 - Example Problems Chapter 7-4

**Example 7.11**

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current *ID* = 0.5 mA. The MOSFET is specified to have *Vt* = 1 V and *kn' W/L* = 1 mA/V2. For simplicity, neglect the channel-length modulation effect (i.e., assume ** = 0). Use a power-supply *VDD* = 15 V. Calculate the percentage change in the value of *ID* obtained when the MOSFET is replaced with another unit having the same *k'n W/L* but *Vt* = 1.5 V.

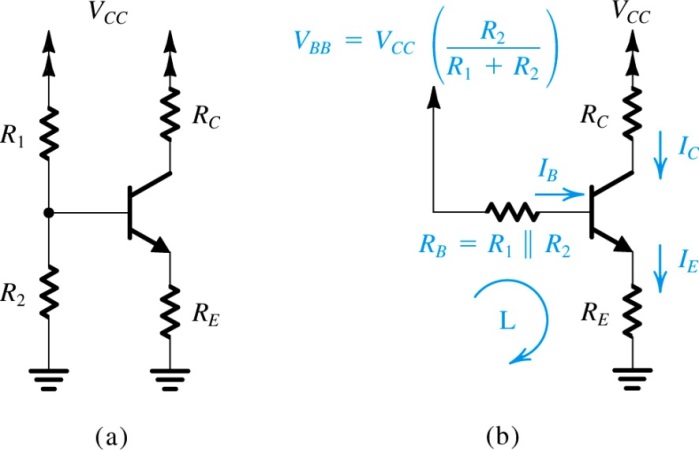


**Figure 7.49** Circuit for Example7.11.

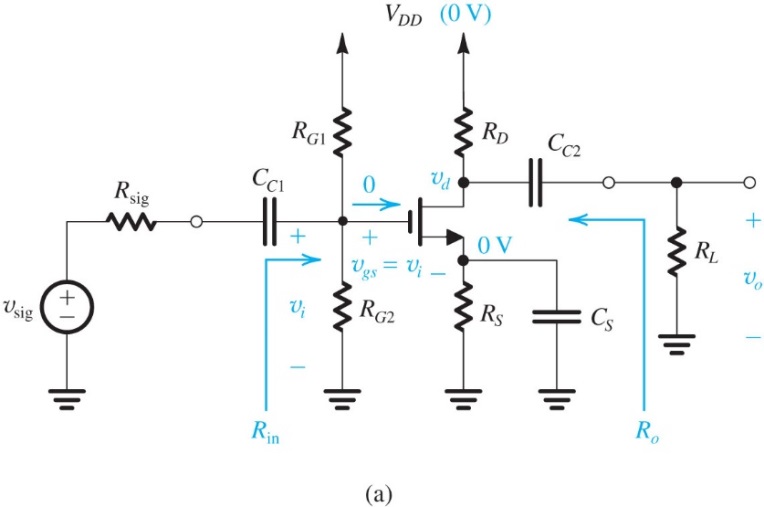
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**Example 7.12**

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current *IE* = 1 mA using a power supply *VCC* = +12 V. The transistor is specified to have a nominal *β* value of 100.



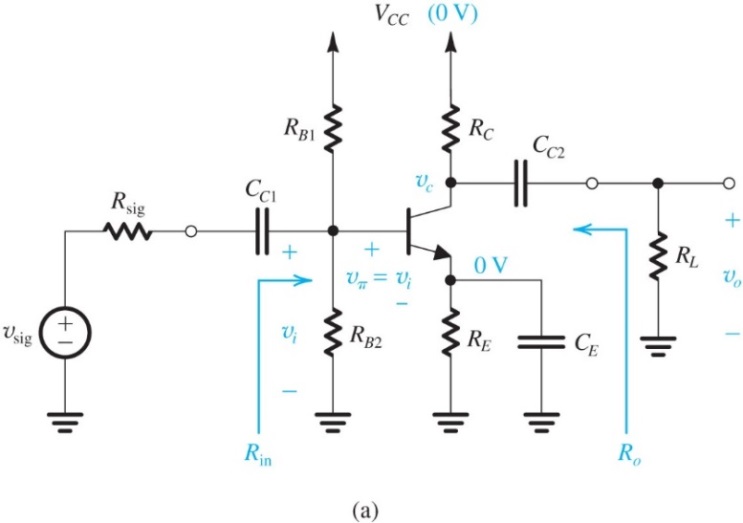
**Figure 7.52** Classical biasing for BJTs using a single power supply: (a) circuit;

**Exercise 7.37**

Design the bias circuit in Fig.7.55(b) for the CS amplifier of Fig. 7.55(a). Assume the MOSFET is specified to have *Vt* = 1 V, *kn* = 4 mA/V2, and *VA* = 100 V. Neglecting the Early effect, design for *ID* = 0.5 mA, *VS* = 3.5 V, and *VD* = 6 V using a power-supply *VDD* = 15 V. Specify the values of *RS* and *RD*. If a current of 2 μA is used in the voltage divider, specify the values of *RG*1 and *RG*2. Give the values of the MOSFET parameters *gm* and *ro* at the bias point.

**Exercise 7.38**

For the CS amplifier of Fig. 7.55(a) use the design obtained in Exercise 7.37 to determine *R*in, *Ro*, and the overall voltage gain *Gv*when *R*sig = 100 k and *RL*= 20 k.

**Exercise 7.40**

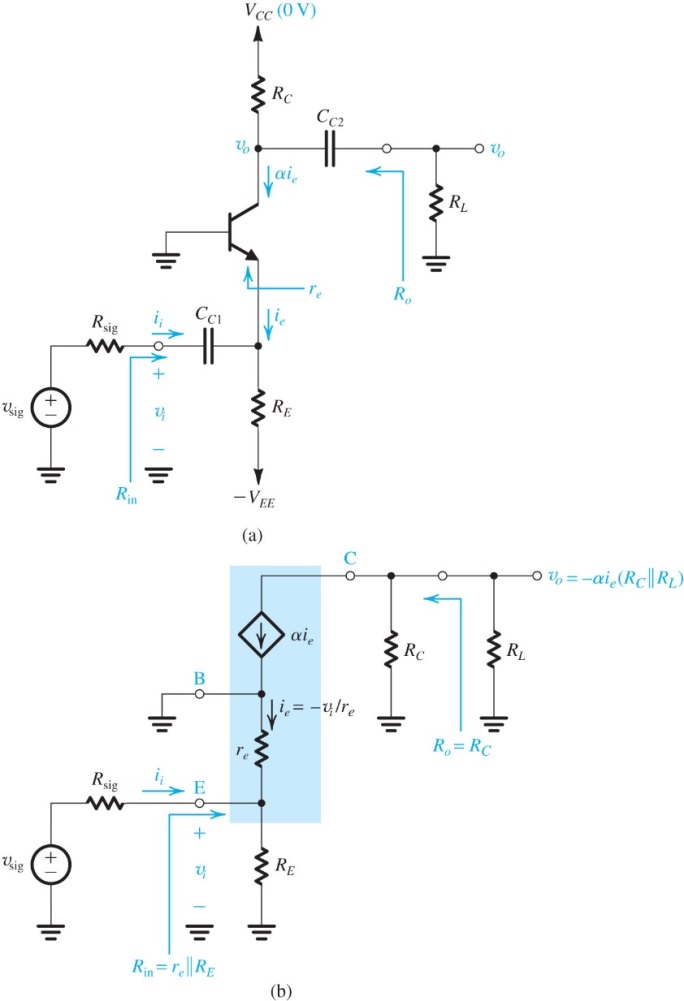
Design the bias circuit of the CE amplifier of Fig. 7.56(a) to obtain *IE* = 0.5 mA and *VC* = +6 V. Design for a dc voltage at the base of 5 V and a current through *RB*2 of 50 μA. Let *VCC* = +15 V, *β* = 100, and *VBE* ≃ 0.7 V. Specify the values of *RB*1, *RB*2, *RE*, and *RC*. Also give the values of the BJT small-signal parameters *gm*, *rπ*, and *ro* at the bias point. (For the calculation of *ro*, let *VA* = 100 V.)

**Exercise 7.41**

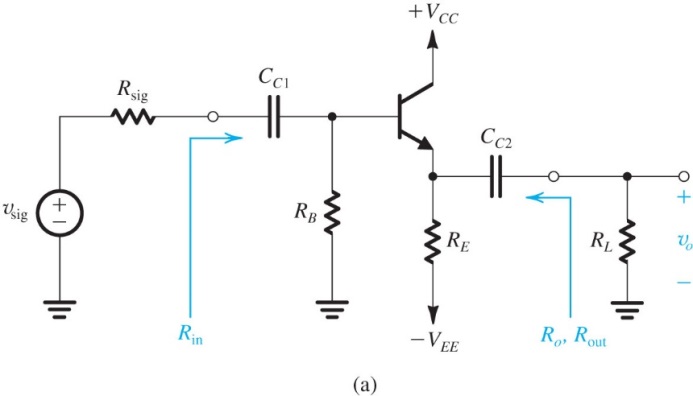
For the amplifier designed in Exercise 7.40, find *Rin*, *Ro*, and *Gv* when *R*sig = 10 k and *RL* = 20 k.

**Exercise 7.42**

For the amplifier designed in Exercise 7.40 and analyzed in Exercise 7.41, let it be required to raise *Rin* to 10 k. What is the required value of *Re*, and what does the overall voltage gain *Gv* become?

**Exercise 7.43**

Design the CB amplifier of Fig. 7.58(a) to provide an input resistance *R*in that matches the source resistance of a cable with a characteristic resistance of 50 . Assume that *RE* ≫ *re*. The available power supplies are ±5 V and *RL* = 8 k. Design for a dc collector voltage *VC* = +1 V. Specify the values of *RC* and *RE*. What overall voltage gain is obtained? If *vsig* is a sine wave with a peak amplitude of 10 mV, what is the peak amplitude of the output voltage? Let α ≃ 1.

**Exercise 7.44**

Design the emitter follower of Fig. 7.59(a) to operate at a dc emitter current *IE* = 1 mA. Allow a dc voltage drop across *RB* of 1 V. The available power supplies are ± 5 V, *β* = 100, *VBE* = 0.7 V, and *VA* = 100 V. Specify the values required for *RB* and *RE*. Now if *R*sig = 50 k and *RL* = 1k, find *R*in, *vi*/*v*sig, *vo*/*vi*, *Gv*, and *R*out. (Note: In performing the bias design, neglect the Early effect.)